

Serial No. 09/710,057

Amendment dated January 8, 2004

Response to Office Action dated October 10, 2003

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Amendments to the Drawings:

Please amend FIG. 1 as shown in the amended drawing page attached hereto to include the following legend: "Prior Art".

Please amend FIG. 2 as shown in the amended drawing page attached hereto to include the following legend: "Prior Art".

Amendments to the Specification:

Please amend the Specification as follows:

Page 15, line 18, delete the blank line after "Ser. No." and replace it with "09/709,855".

Page 15, line 19, delete ", now U.S. Pat. No. _____,".

Page 16, line 22, delete the blank line after "Ser. No." and replace it with "09/709,801".

Page 17, line 2, delete the blank line after "Pat. No." and replace with "6,606,721".

Amendments to the Claims:

Please amend the claims as follows (it being understood that the following listing of claims will replace all prior versions and listings of claims in the application):

Listing of Claims:

1. (currently amended). A processor verification test apparatus that uses a golden model to generate a test program that verifies that a processor system under test properly executes two or more instructions issued and executed in parallel, comprising: